Josephson Microprocessors

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ABSTRACT. The Josephson microprocessor is a good example for exhibiting typical performance of digital circuits with Josephson devices. Although present Josephson microprocessors are not large, they can be operated over ten times faster than similar semiconductor microprocessors. This kind of performance is due largely to the reliability of Josephson junction technology. The niobium Josephson junction (Nb/AlOx/Nb) has served as the base upon which high-speed digital circuits have been developed because of its uniform, stable characteristics. Using niobium junctions, we can fabricate microprocessors having a few thousand gates and memory of a few kilobits. Interface circuits to adapt the Josephson circuit signal to semiconductor circuits are also feasible. Josephson microprocessor development, as described in this paper, relies mainly on the technology for niobium junction fabrication, the high-speed logic gate family, and the power system. An experimental cryogenic system for a prototype Josephson computer is also described.

1. Introduction

Thirty years have passed since B. D. Josephson announced his theory on the tunneling effect that came to bear his name (Josephson (1962)), [1]. Over the years, a variety of applications using Josephson devices has been proposed and developed. Examples include the highly sensitive magnetic sensor called the superconducting quantum interference device (SQUID), voltage standards, and electromagnetic detectors. An as yet immature but important application is digital circuits with Josephson devices, but this has yet to reach practical use. State-of-the-art technology is at a level where prototype integrated circuits, such as microprocessors having a few thousand gates and memory of a few kilobits, are possible. Although not as sophisticated as comparable semiconductor technology, Josephson digital technology has the potential to overcome the limits of semiconductor technology due to the sheer speed of such circuits.

This paper describes the present status of Josephson processor technology, typified by 4-bit microprocessors and 8-bit digital signal processors (DSPs), together with the techniques to fabricate these microprocessors, i.e., (1) the fabrication of very reliable niobium junctions, (2) the high-speed-logic gate family, and (3) a power system suited to high-speed operation. This paper also provides an introduction to the basic principles for Josephson logic and memory, and describes future directions for Josephson digital technology.

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2. Logic and Memory Operation

Figure 1 shows Josephson-junction current-voltage (I-V) characteristics: (a) illustrates the operating regions and (b) shows actual characteristics. The junction has two stable states: superconducting, with no voltage across the junction; and voltage, with gap voltage V_g. Logic state 0 is assigned to the superconducting state and logic state 1 to the voltage state. When input signals are applied, the superconducting state switches to the voltage state along the load line, as will be shown later. V_g, usually a few mV, is determined by the junction material. For a niobium junction, V_g is 2.8 mV.

Josephson logic gates are classified into two types: magnetic-coupled and current-injected. In the magnetic-coupled gate, the input signal current magnetically couples to the gate, reducing the maximum supercurrent flowing through the gate and switching to the voltage state. In the current-injected gate, the input current is directly injected into the gate, causing the gate junction to switch to the voltage state, but not isolating the input signal current from the output. Thus, to prevent the input signal current from flowing to the output terminal, an additional junction and resistor are connected to the gate junction for isolation.

Among the Josephson logic gates proposed, Josephson interferometer logic (JIL) (Klein and Herrell (1978)), [2], resistor-coupled Josephson logic (RCJL) (Sone et al. (1982)), [3], four-junction logic (4JL) (Takada et al. (1979)), [4], and modified variable threshold logic (MVTL) (Fujimaki et al. (1989)), [5] gates are now used in high-speed circuits. Of these, the fastest switching speed (1.5 ps/gate) has been recorded with the MVTL OR gate (Kotani et al. (1988)), [6], described later. Figure 2 shows equivalent circuits for JIL, RCJL, 4JL, and MVTL gates. Each functions as an OR gate. JIL is controlled using a magnetic field generated by the input signal current. RCJL and 4JL are controlled using a directly-injected input signal current. MVTL uses both magnetic coupling and current injection.

Figure 3 shows simulation waveforms for JIL gate operation: (a) shows the movement of the operating point on the I-V characteristics; (b) the threshold characteristic, i.e., how critical threshold current I_C changes with the input signal current; (c) the bias current waveform I_B; (d) the input signal current I_{in}; and (e) the junction voltage V_J. When the bias current is supplied to the gate, the operating point moves from origin O to point A, where the gate stands by for switching to voltage state B. When I_B is below critical current I_C, the junction is in the zero voltage state at operating point A. Applying input signal I_{in} to the gate generates a magnetic field that is coupled to the gate inductance and reduces I_C. When I_C drops below I_B, the gate switches to the voltage state at operating point B. The operating point then remains at B, even if I_{in} is removed. The gate is reset only by decreasing I_B. The operating point goes from O to A, to B, and back to O. If the input signal is zero, I_C does not drop below I_B, and the operating point remains at A. The operating point only returns to O when I_B is turned off, i.e., the operating point thus moves simply from O to A, then to O.

The gate's switching time is determined primarily by CR, where C is the junction capacitance and R is the impedance of the strip line, which is usually chosen to match the tunneling resistance. The junction capacitance per unit area is 0.06 pF/μm^2 for the niobium junction (Kotani et al. (1986)), [7]. For a logic gate with junctions of a few μm, the junction capacitance is on the order of 1 pF. R is usually several ohms, resulting in a switching time of several ps. Actually obtained switching time is discussed later.

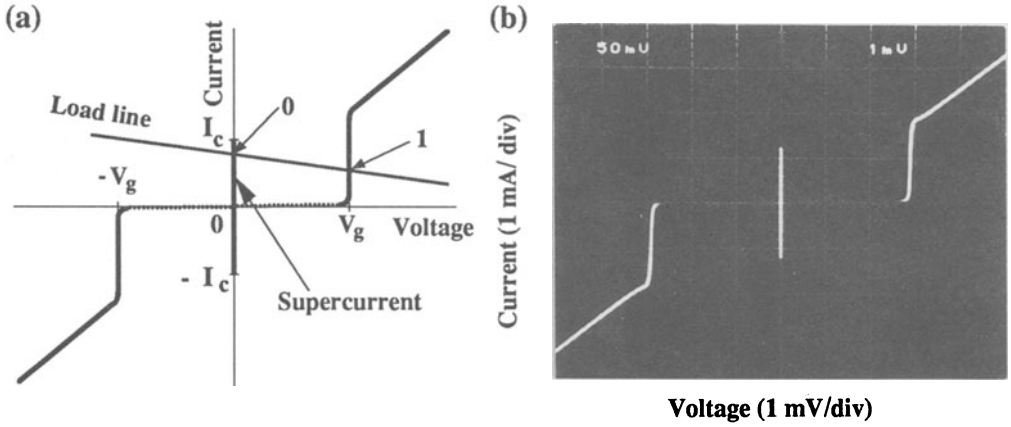


Fig. 1 Josephson junction I-V characteristics. (a) Schematic. The bold central line shows supercurrent. (b) Actual oscilloscope I-V curve for a typical junction.

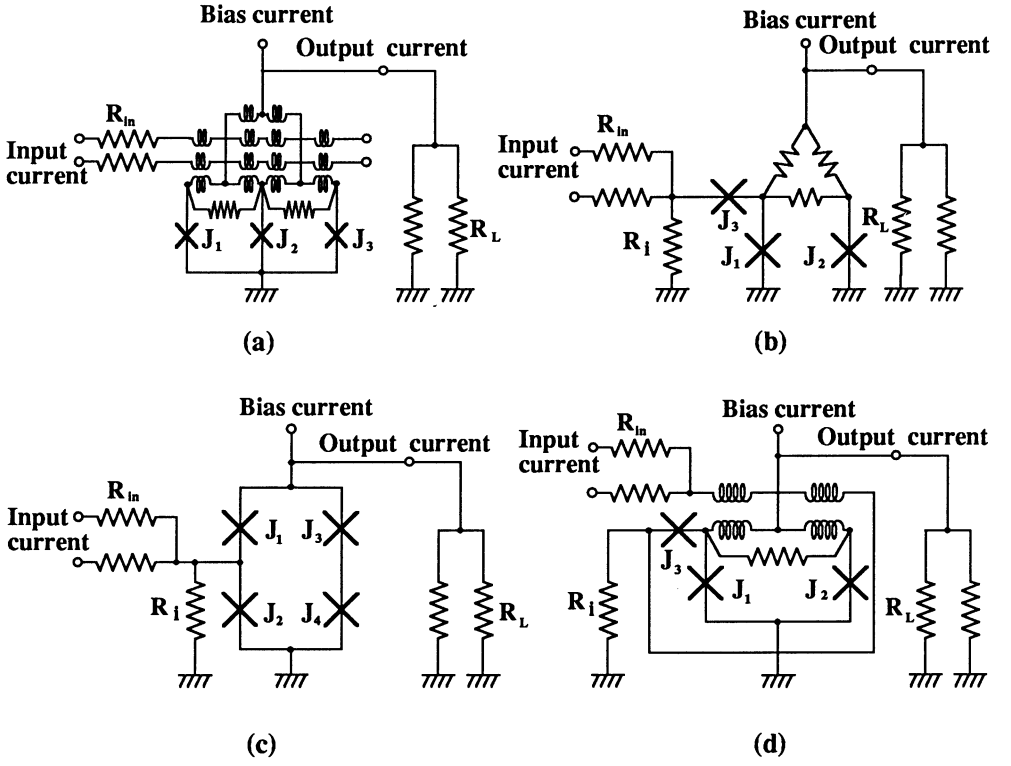


Fig. 2 Equivalent circuit of logic gates. (a) JIL, (b) RCJL, (c) 4JL, (d) MVTL.

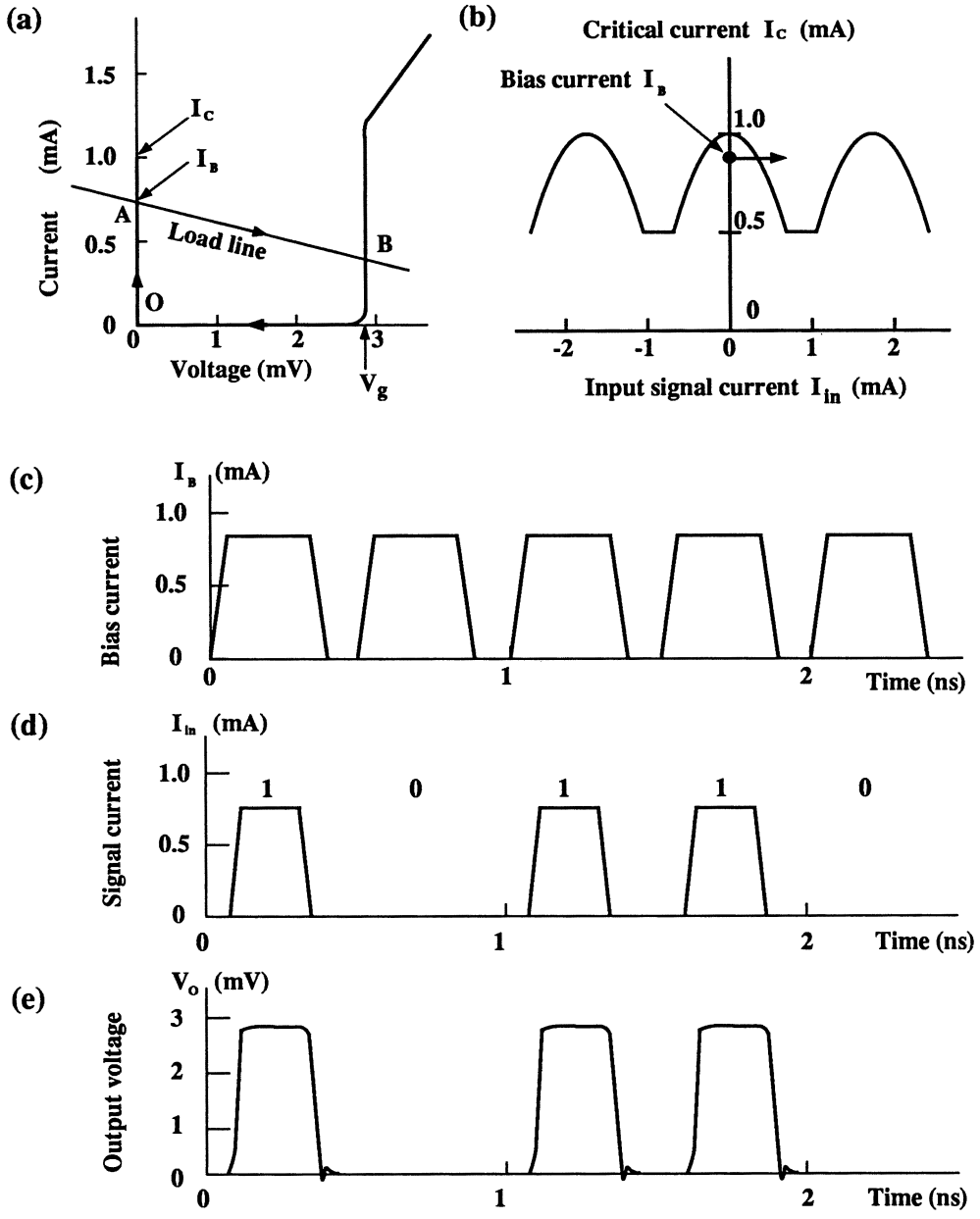


Fig. 3 Computer-simulated JIL gate switching. (a) I-V characteristics. (b) Threshold characteristics. (c) Bias current. (d) Input signal current. (e) Output voltage.

The basic concept behind Josephson memory is to store information as a persistent supercurrent flowing in a ring of superconducting wire. Usually, the ring contains one or two Josephson gates which control the current flow. The magnetic flux caused by the persistent current is quantized in units of flux quantum Φ_0. Φ_0 has a value of h/2e (= 2.07 x 10^{-15} Wb), where h is Planck's constant and e is the electronic charge. Although semiconductor dynamic memory stores a few hundred thousand electrons in a capacitor cell, Josephson memory stores only one or two flux quanta in the ring.

Stored information in the superconducting ring is read using another logic gate which senses the persistent supercurrent and switches to the voltage state. Readout methods are classified into two types: destructive and nondestructive. Destructive readout means that the persistent current disappears when it is sensed by the readout gate, while nondestructive readout maintains persistent current in the same state as before. For destructive readout, information should be rewritten immediately following the readout.

Figure 4 shows equivalent circuits for all Josephson memory cells reported. These include (a) the conventional cell developed by H. Henkels (Henkels (1979)), [8], (b) the variable threshold cell developed by I. Kurosawa (Kurosawa et al. (1989)), [9], (c) the vortex transitional cell developed by S. Tahara (Tahara et al. (1991)), [10], and (d) the capacitively-coupled cell developed by H. Suzuki (Suzuki et al. (1989)), [11]. The first three involve nondestructive readout, and the fourth uses destructive readout.

3. Integrated circuit fabrication

As shown in Fig. 1, Josephson junctions with an Nb/AlOx/Nb structure exhibit excellent characteristics. The niobium junction was first developed by M. Gurvitch et al. of AT&T Bell Laboratories in 1983 (Gurvitch et al. (1983)), [12]. Its properties are very stable against thermal cycling and long-term storage at room temperature. Junction critical-current scatter is quite small, and is both reproducible and controllable.

The niobium-aluminum combination is required to obtain high-quality junctions. Figure 5 shows a cross-sectional transmission-electron-microscope (TEM) photograph of a Nb/AlOx/Nb junction's lattice (Imamura and Hasuo (1991)), [13]. Nb and Al are deposited on wafers attached to a water-cooled wafer holder. The upper Nb layer is 20-nm thick, and the lower one is 200-nm thick. The Al is 14-nm thick. The lower Al and Nb interface is rough and wavy due to the rough Nb surface. The other interface, between the upper Nb and AlOx, is sharp and clear, indicating that Al planarizes the lower Nb surface. Consequently, the planarized Al surface is considered essential for growing a pinhole-free AlOx barrier. TEM studies indicate that the Nb, Al, and AlOx combination is nearly ideal for Josephson junctions--the main reason why one obtains high-quality Josephson junctions with the Nb/AlOx/Nb structure.

Nb/AlOx/Nb junctions are very stable in thermal cycling between liquid helium and room temperature. They are also stable in room temperature storage. I-V characteristics were found unchanged after five years of room temperature storage (Morohashi et al. (1991)), [14].

A typical Josephson circuit consists of a Nb ground plane, Mo resistors, a SiO or SiOx (Shibayama et al. (1985)), [15] protective layer for resistors, Nb/AlOx/Nb Josephson junctions with Nb base and counter electrodes, SiO_2 insulation layers, Nb wiring, and a Nb control line, as shown in Fig. 6. Layer material and thickness are summarized in Table 1 (Imamura (1991)), [16]. Eight to 11 photomasks are usually used to fabricate circuit patterns. Circuits can be

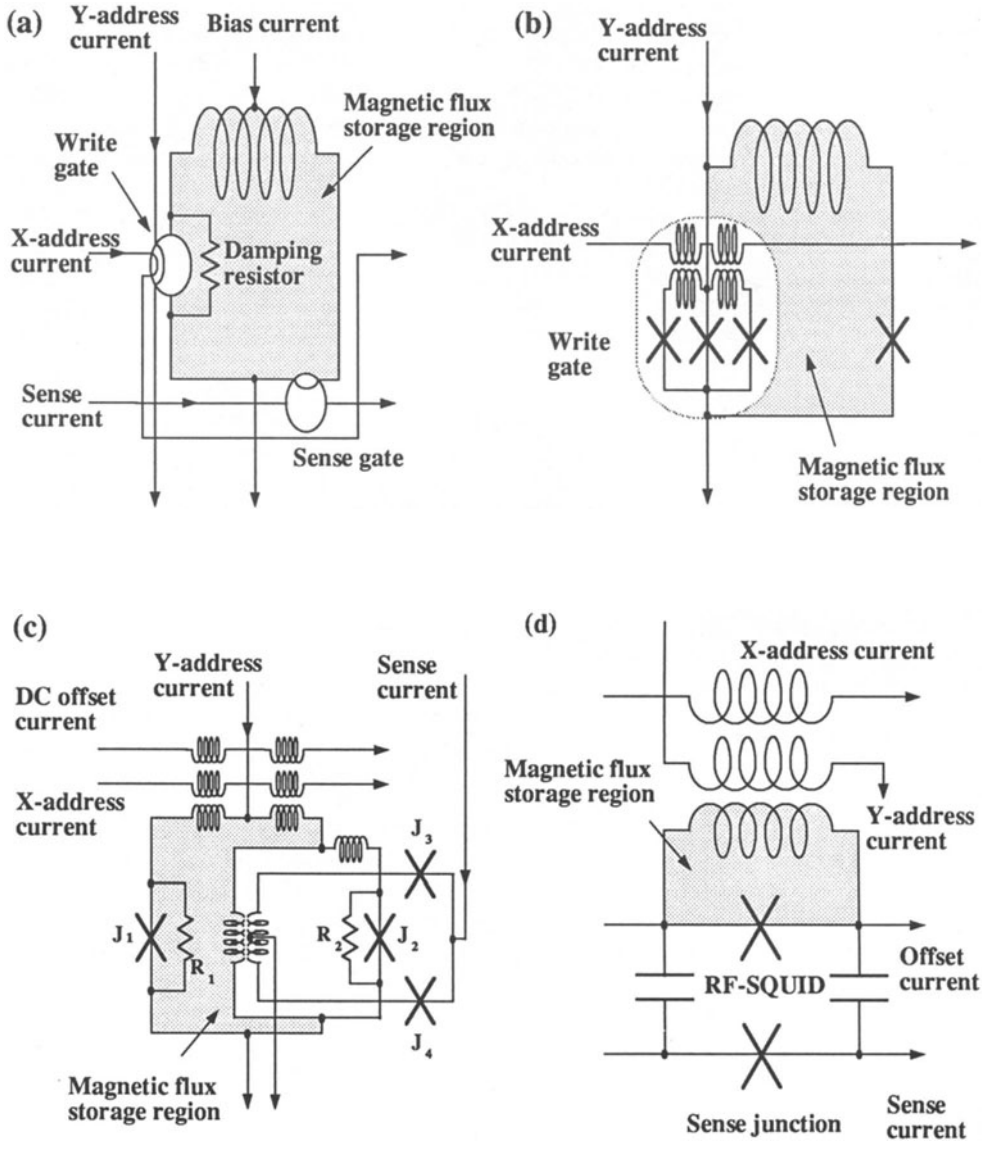


Fig. 4 Equivalent circuits for Josephson memory cells. (a) Conventional Henkels type. (b) Variable threshold. (c) Vortex transition. (d) Capacitively coupled.

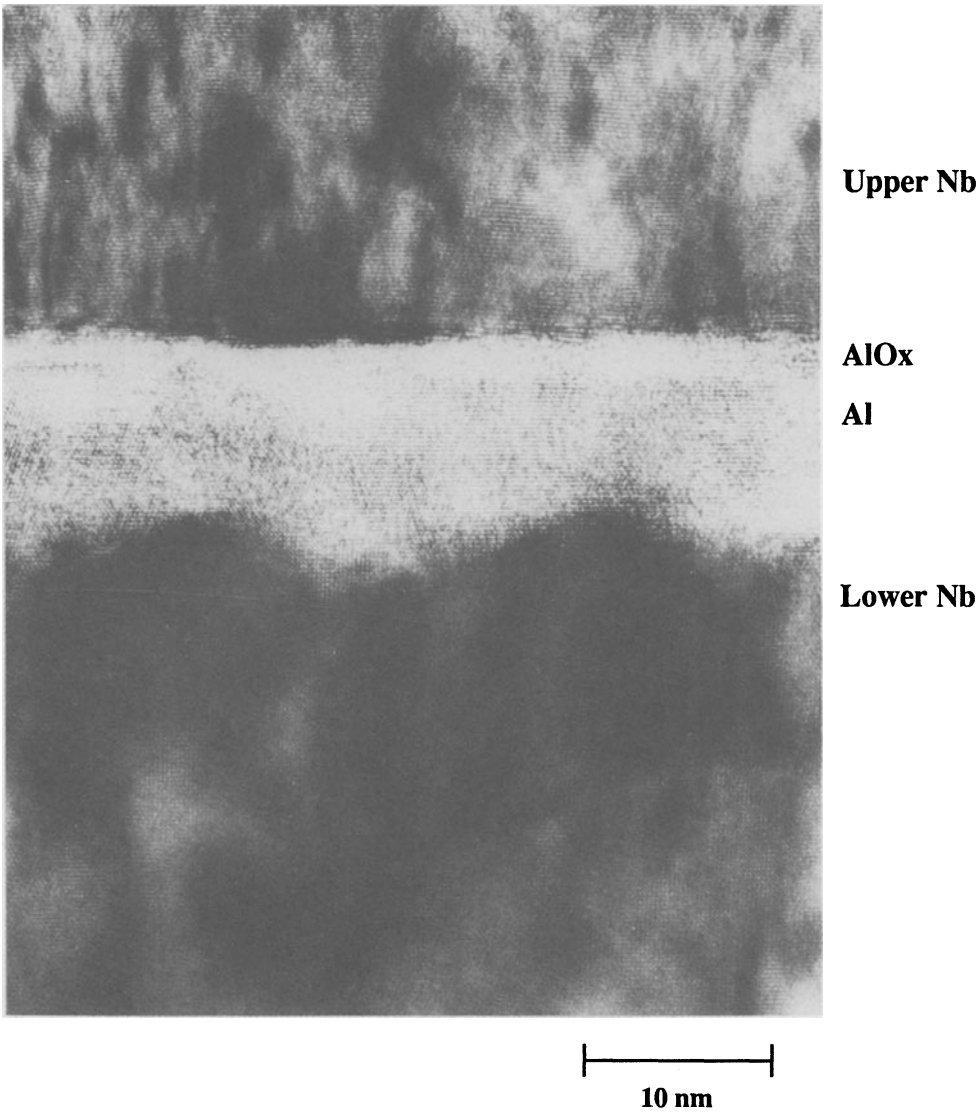


Fig. 5 Cross sectional TEM image of Nb/AlOx/Nb junction, where AlOx consists of aluminum oxide formed on a sputter-deposited thin aluminum layer.

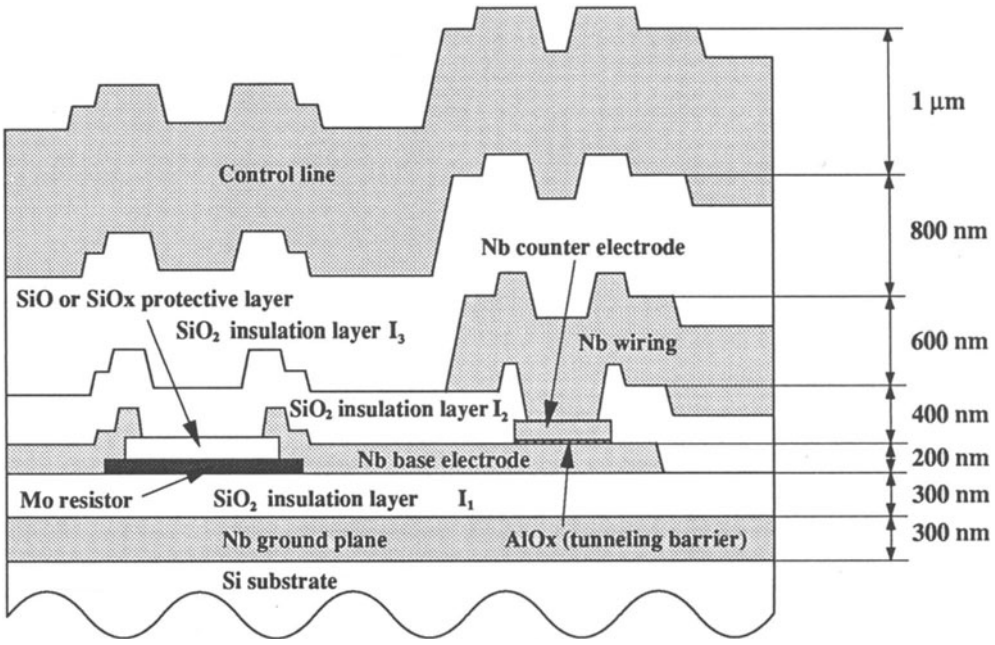


Fig. 6 Typical Josephson circuit with Nb/AlOx/Nb junctions.

Table 1 Circuit layers

Symbol	Name	Material	Thickness (nm)
GP	Ground plane	Nb	300
I_1	Insulation	SiO_2	300
R	Resistor	Mo	100
P	Resistor protection	SiO or SiO_x	100
B	Base electrode	Nb	200
T	Tunneling barrier	AlOx-Al	7
C	Counter electrode	Nb	100-200
I_2	Insulation	SiO_2	400
WR	Wiring	Nb	600
I_3	Insulation	SiO_2	800
CL	Control line	Nb	1000

stacked on any flat substrate material. Silicon is usually used, however, so conventional semiconductor manufacturing equipment can be employed.

Nb, Al, Mo, and SiO_2 are deposited by sputtering (Table 2). The SiOx protective layer is deposited by evaporating SiO in an oxygen atmosphere (Shibayama et al. (1985)), [15], and protects resistors during reactive ion etching (RIE) of the Nb base electrode. Except for the protective layer, all layers are patterned by RIE. Table 3 lists the reactive gases used in etching. Al and AlOx act as etch stoppers because they are not etched by reactive CF_4 or CHF_3. The thin AlOx-Al barrier is removed by Ar sputter etching. The SiOx is patterned by liftoff.

The most important process in fabricating uniform junctions is making a uniform thin tunneling barrier. Several nanometers of Al are deposited on a Nb base electrode. The Al surface is oxidized by introducing a gaseous mixture of 90% Ar and 10% O_2, then Nb is deposited to make a counter electrode. These processes are done in the same vacuum chamber to avoid exposing wafers to air, enabling uniform junction characteristics to be obtained for the entire wafer. The junction's critical current density, j_C, is determined by controlling the oxidation gas pressure from 50 to 200 Pa and the oxidation time from 30 to 60 minutes. j_C is controlled from 1 to 10^4 A/cm^2.

Figure 7 (a) shows the MVTL OR gate. The doughnut-like structures are formed by the junction (outer perimeter) and the contact "doughnut" hole. Junctions J_1, J_2, and J_3 are used for one gate. The gate cross section in Fig. 7 (b) has been exaggerated horizontally to emphasize the junction structure. The control line and I_3 layers are not used here, since the wiring layer also provides control lines for magnetic coupling, simplifying fabrication. The sequence for MVTL gate fabrication is shown in Fig. 8.

Circuits are usually fabricated above a superconducting ground plane. The base, wiring, and control-line layers form microstrip lines, enabling high-speed signal transmission on the chip. Microstrip lines are usually 2-to-3-μm wide and have a characteristic impedance of about 10 Ω.

4. Gate Families

As discussed in Section 2, a variety of logic gates has been proposed, each having its own logic family. Josephson logic-gate families usually consist of OR, AND, majority (MJ), and timed-inverter (TI) gates. Using these gates, we can construct any kind of circuit.

This section discusses the MVTL family of OR, AND, 2/3 MJ, and TI gates.

4.1. OR GATE

The MVTL OR gate (Fig. 2(d)) is the most important member of this family because, in addition to providing the OR function, it isolates input and output signals in the AND, 2/3 MJ, and TI gates.

The MVTL OR gate was designed to have a large operating margin and high sensitivity to the input signal current, this latter feature making it usable as a high-speed gate. It is basically a two-junction interferometer or SQUID.

In the gate, the critical current for J_1 is pI_m and that for J_2 is qI_m, where p and q are fractions whose sum is one, and I_m is the SQUID's maximum supercurrent. Inductance L is coupled magnetically to control-line inductance L_x through mutual inductance M. Bias current I_B is applied to the point between the left-branch inductance qL and the right-branch inductance pL,

Table 2 Sputtering conditions for metal and insulation layer

Material	Ar pressure (Pa)	Deposition rate (nm/min)
Nb	1.3 - 2.3	200
Al	1.3	8
Mo	0.67	130
SiO_2	1.3	8

Table 3 Metal and insulation layer patterning

Material	Reactive gas	Pressure (Pa)	Power density (W/cm^2)
Nb	CF_4(5 - 20 % O_2)	2.7 - 6.7	0.10
Al	Ar	0.7	0.15
Mo	CF_4(5 % O_2)	6.7	0.10
SiO_2	CHF_3(0 - 15 % O_2)	2.0	0.20

(a)

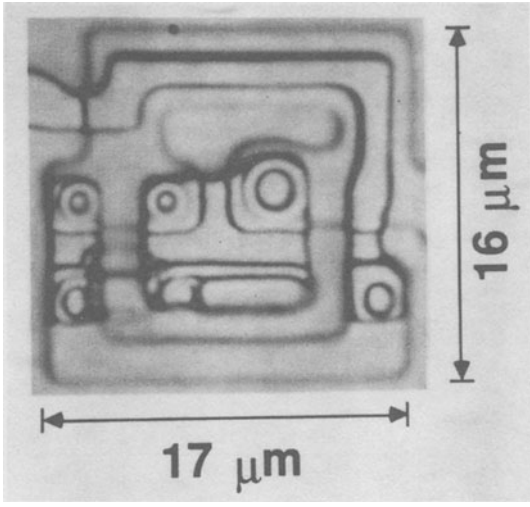
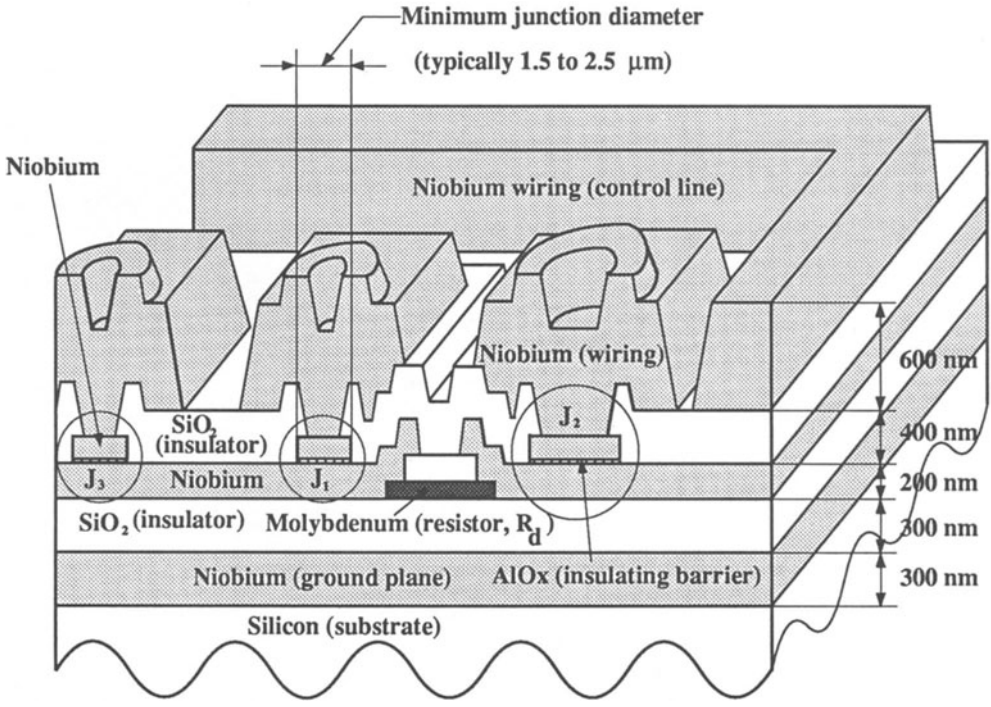
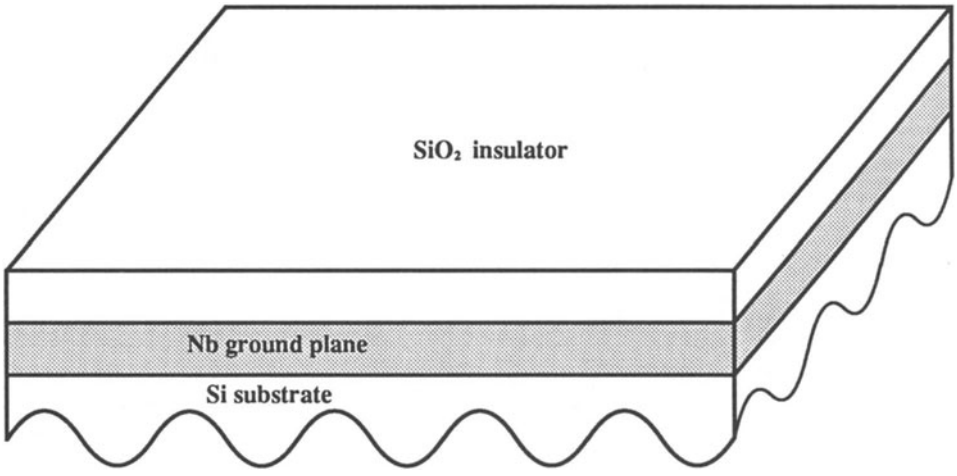


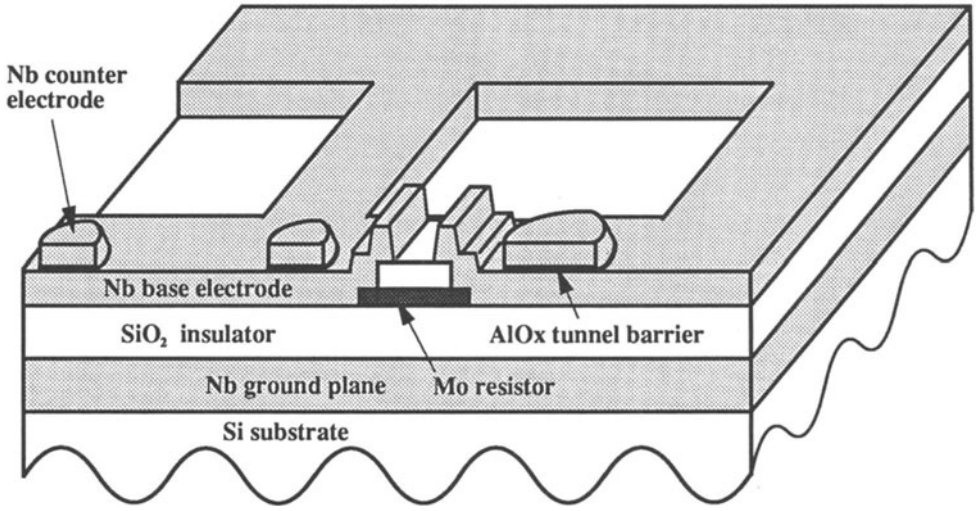
Fig. 7 (a) (Left) MVTL OR gate with a minimum junction diameter of 1.2 μm. (b) (Below) Gate cross section. Doughnut-like structures are Nb/AlOx/Nb junctions. Here, the minimum junction diameter, J_1 is 1.2 μm in the case of the gate in (a), but it is typically 1.5 to 2.5 μm for the actual circuits.

(b)



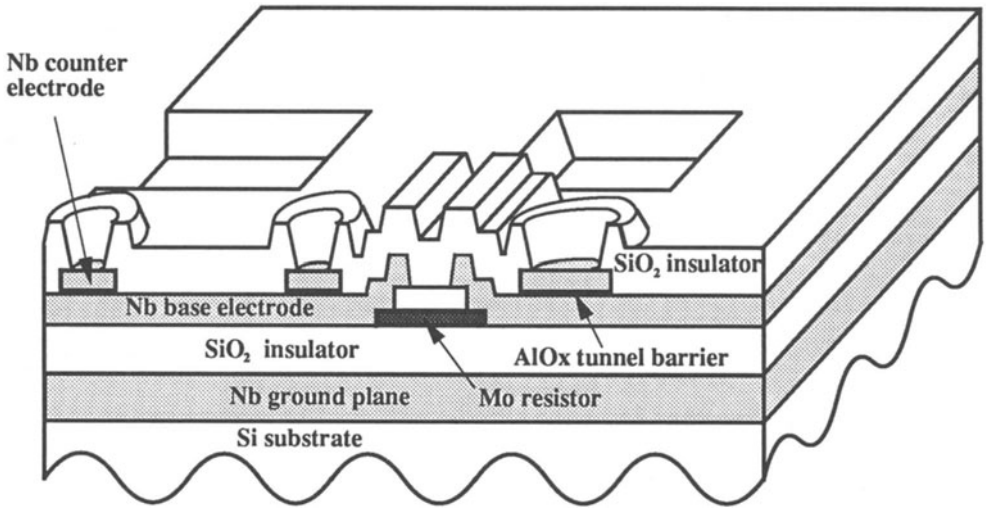


(a) Ground plane and insulating layer deposition

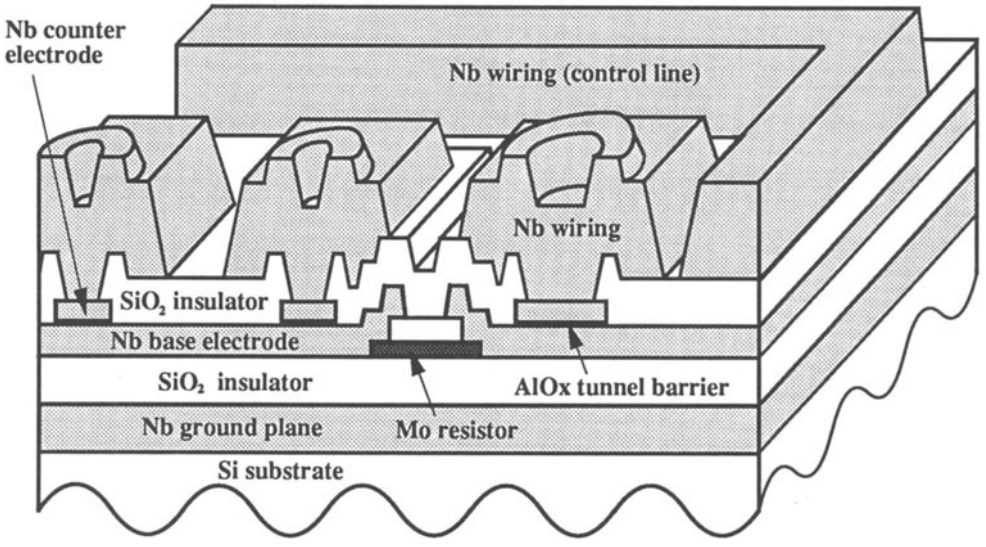


(b) Deposition and patterning of resistor and junction

Fig. 8 Fabrication sequence of the MVTL OR gate.



(c) Deposition and patterning of insulation layer



(d) Deposition and patterning of wiring layer

Fig. 8 Fabrication sequence of the MVTL OR gate (continued).

ensuring that the bias current's upper limit is I_m. The input-signal current is fed through L_x and applied to the SQUID. A damping resistor R_d is used in parallel with inductance L to prevent resonance between L and junction capacitance C.

When bias and input currents are applied and the operating point crosses the interferometer's threshold, junctions J_1 and J_2 switch. The bias current then flows through J_3 and R_i to ground. J_3 is switched to the voltage state and almost all of the bias current flows to load resistor R_L. After the gate switches to the voltage state, the input current flows through R_i to ground, isolating the input and output signals. Optimized gate parameters are listed in Table 4 (Fujimaki et al. (1989)), [5]. The operating margin of the bias current is ±43% for the optimized gate.

In semiconductor circuits, ring oscillators are used to measure switching delay. In Josephson circuits, which have no inverter gate without using a timing signal (discussed later), the switching delay is usually measured using a gate chain of multiple logic stages. In Fujitsu's circuit, 101 gates are connected to measure the total switching time for 100 stages.

The critical currents of gate junctions J_1, J_2, and J_3 are designed to be 0.1, 0.3, and 0.1 mA. We fabricated five gate types with different junction sizes, (4, 7, 4), (2.5, 4.3, 2.5), (2, 3.5, 2), (1.5, 2.6,1.5), and (1.2, 2, 1.2) μm diameters for (J_1, J_2, J_3). For these five gates, I_m was kept unchanged. Thus, the smaller the gate junction, the higher the critical current density. The fastest switching speed, 1.5 ps/gate, was obtained using a gate with a minimum junction (J_1) diameter of 1.2 μm (Kotani et al. (1988)), [6]. The power consumption for the 1.5 ps/gate was 12 μW/gate. The gate chain operated correctly for a bias current margin of ±20%, reduced from the design value of ±43% because of critical current scattering and other process-dependent parameters in the chain.

In the fastest switching delay times for different minimum junction diameters (Fig. 9), the switching delay is almost proportional to the minimum junction diameter, suggesting that subpicosecond switching is feasible with submicron-diameter junctions.

4.2. OTHER MVTL GATES

The MVTL AND gate is constructed using a single junction. Critical current I_a of AND junction J_a is designed so that the junction can be switched when the sum of the two input currents exceeds I_a. Because this junction cannot isolate output from input signals, it is usually used after an OR gate (Fig. 10 (a)), in a configuration we call a 2OR-AND gate. To prevent J_a from being switched by leakage current from the next-stage gate, J_a is connected to resistor R_p and junction J_p. The critical current of junction J_p equals that of the OR gate, and is small enough to minimize current loss through J_p when switching to the voltage state. The 2/3 MJ gate (Fig. 10 (b)) outputs a value of 1 if two or three of the three input signals are 1. Otherwise, the output is 0. The bias current operating margin for both the 2OR-AND and 2/3 MJ gates is ±33%.

Latching characteristics prevent the Josephson junction from being used to construct inverters. Because the gate requires a timing signal for inversion, an inverter gate or a timed-inverter (TI) gate must be constructed using a timing signal (Fig. 11). The inverter operates correctly when the signal current is applied just before the bias current rises.

Table 5 summarizes MVTL gate performance (Fujimaki et al. (1989) and Kotani et al. (1988)), [5, 6]. Since the performance of the 2OR-AND and 2/3 MJ gates can be estimated from OR gate data, we have not fabricated test gates for junction diameters such as 2.0 and 1.5 μm.

Table 4 Optimized MVTL OR gate parameters

Parameter	Optimized value
Maximum supercurrent: I_m	0.4 mA
Inductance: L	5.2 pH
LI_m product: LI_m / Φ_0	1.0
Division ratio of L or I_m : q / p	3
Mutual inductance: M	0.8 L
Control line inductance: L_x	3-5 L
Isolation resistor: R_i	1 Ω
Damping resistor: R_d	1.8 Ω

Φ_0: flux quantum (2.07 x 10^{-15} Wb)

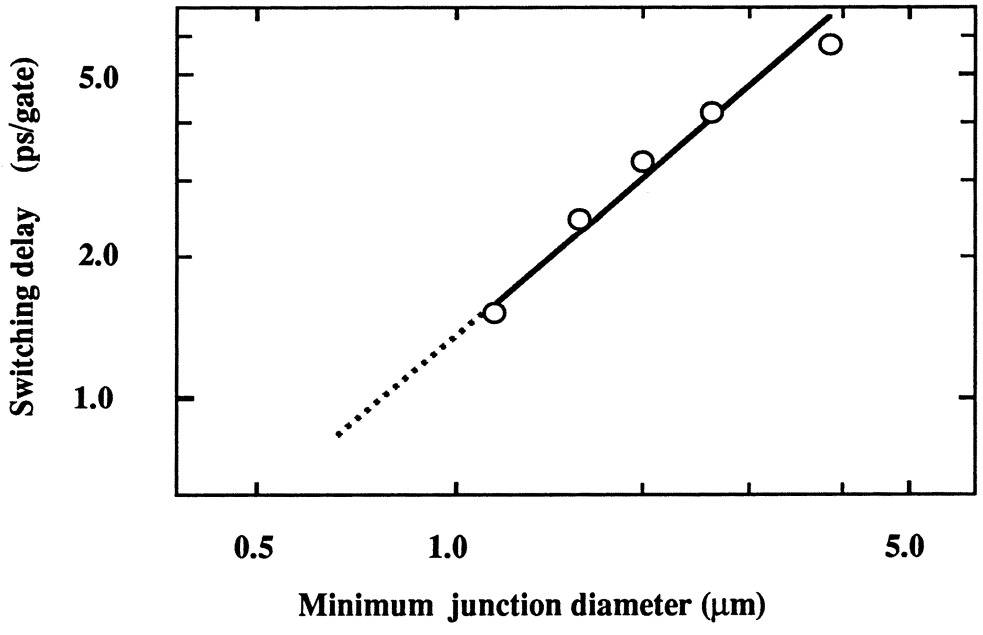


Fig. 9 Fastest gate delay and minimum junction diameter.

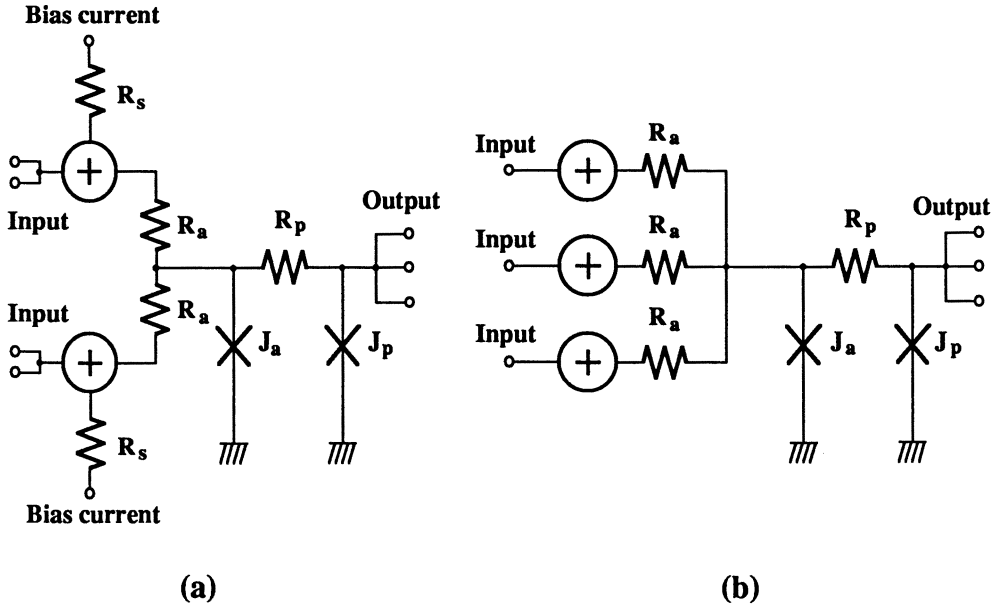


Fig. 10 Equivalent circuits. (a) 2OR-AND (unit cell) gate. (b) 2/3 MJ gate.

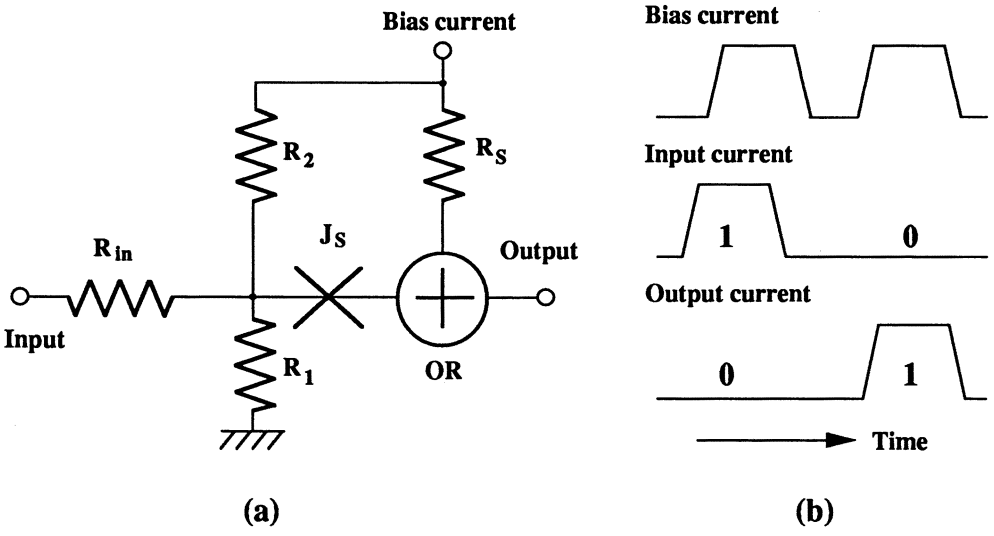


Fig. 11 Timed inverter gate. (a) Equivalent circuit. (b) Timing sequence.

The TI gate delay is not given here because a timing signal is required and the gate delay depends on this timing signal.

5. JJ Device Power System

As discussed in Section 2, Josephson devices operate in a latching mode, requiring a different power system from that for semiconductor devices. Bias currents for Josephson devices are supplied by pulse rather than dc power, requiring special techniques to ensure their performance potential.

Josephson logic gates switch to the voltage state only when an input signal is applied. Once switched, the gate voltage does not return to zero, even after the input signal is turned off. The power supply for Josephson logic gates must thus be turned off to reset the gate in each clock cycle. Sinusoidal ac power is thus supplied from an external source and is made trapezoidal using a regulator circuit (Fig. 12) (Arnett and Herrell (1979)), [17]. The regulator usually consists of four Josephson junctions connected in series. It generates a clipped waveform and supplies bias current to the gates. Logic operation is executed in the flat part of the source power. Due to the symmetrical current-voltage characteristics of Josephson junctions, both positive and negative bias currents can be used for logic operations.

Note that in conventional power supplies, information must be retained while the bias current is turned off. A special circuit called a latch is used to hold information when the polarity of the bias current changes (Davidson (1978)), [18]. Although the latch uses persistent current to store information in the superconducting loop without bias current, the latch circuitry is rather complicated.

At Fujitsu we developed a new power supply which does not use latches. The three-phase power system, as we call it, uses three dc-offset sinusoidal waveforms, each 120° out of phase. No regulator junctions are used, and the sinusoidal waveform is applied to gates as is. Using a sinusoidal rather than trapezoidal waveform reduces the operating margin. Fortunately, the reduction is only about 10% and is not critical to circuit operation.

Logic operation (Fig. 13) is as follows: When a logic operation is executed and completed in phase ϕ_1, data is transferred to the circuits driven by phase ϕ_2 and processed there. After ϕ_2 is completed, data is sent to the circuits driven by ϕ_3. Data is transferred from circuits in ϕ_3 to those in ϕ_1. This completes one clock cycle. This system requires no latching because processed data is transferred cyclically without wasting time.

TI gates are usually used at each rising edge of the power waveform in the three different phases, since an input signal must be followed by bias current in the TI gate. Complementary data signals can thus be generated three times in one clock cycle. Signal processing in each phase is executed by dual-rail logic (Gheewala (1979)), [19], which uses true and complementary signals for calculation.

One of the important effects of the three-phase power system is the absence of ground-level voltage variation. In chip operation, bias current flows through the bonding wires--or the solder bumps for flip-chip bonding--and is terminated at the common superconducting ground plane. If bias current flowing into the ground plane changes with time, ground-level voltage difference V_{gr} between the chip and circuit board changes greatly. V_{gr} is expressed by L(dI/dt), where I is the total bias current and L the inductance of the bonding wires or flip-chip bonding solder bumps. The clock frequency is about 1 GHz, and the total bias current is about 1 A for a chip with several thousand logic gates. For an L of 50 pH, which is a typical value of flip-chip

Table 5 MVTL gate family performance

Minimum junction diameter (μm)	4.0	2.5	2.0	1.5	1.2
OR	5.6	4.2	3.3	2.5	1.5
2OR-AND	16.0	11.5	—	—	—
2/3 MJ	21.0	—	—	—	—

Unit: ps/gate or ps/unit cell

Note: TI gate delays are not listed because they depend on signal timing.

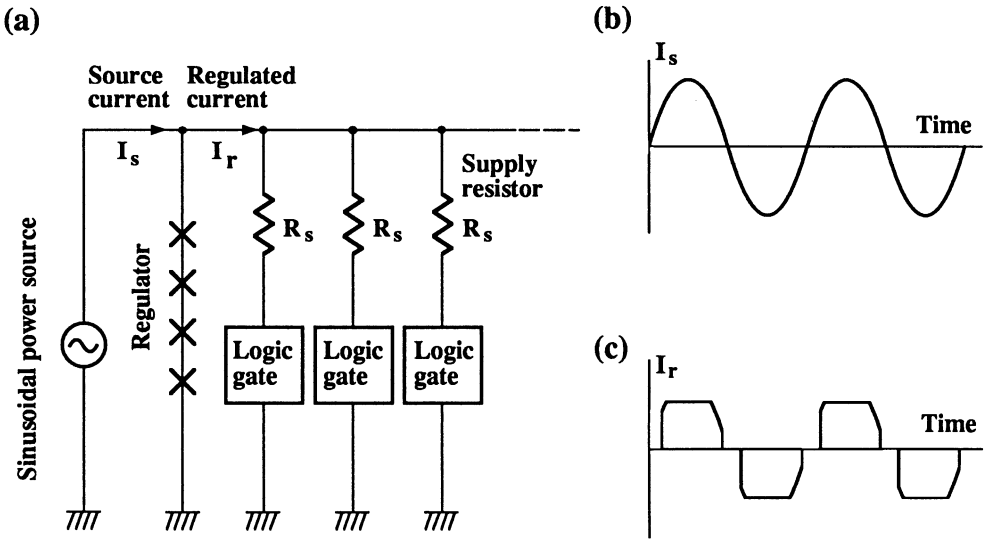


Fig. 12 Conventional power system. (a) Circuit diagram. (b) Current waveform from a sinusoidal current. (c) Current waveform from a regulator.

bonding, V_{gr} is 300 mV and is much larger than the signal voltage of 2.8 mV from a Josephson logic gate. For the three-phase power system, however, all the bias current flowing into the ground plane is dc and does not change with time because of the out-of-phase bias current. Thus, ground-level voltage is not affected by the bias current--a significant advantage which enables Josephson logic circuits to operate at high speeds. Note, however, that the number of gates driven by each phase should be designed to be as equal as possible. Otherwise, the total bias current would change with time, varying the ground-level voltage.

6. Microprocessors

Josephson technology is now at a level where 4-bit or 8-bit microprocessors are possible. Examples of microprocessors using niobium junctions include a 4-chip, 4-bit computer (ETL) (Takada et al. (1991)), [20], a 4-bit data processor (Hitachi) (Hatano et al. (1989)), [21], a 4-bit microprocessor (Fujitsu) (Kotani et al. (1988)), [22], a 4-bit processor (Fujitsu) (Kotani et al. (1990)), [23], and an 8-bit digital signal processor (DSP) (Fujitsu) (Kotani et al. (1990)), [24]. The 4-bit microprocessor, the 4-bit processor, and the 8-bit DSP are discussed in the sections that follows.

6.1. 4-BIT MICROPROCESSOR

The Am2901 microprocessor (Mick (1975)), [25] developed by Advanced Micro Devices Inc. is a world-standard bit-slice microprocessor for which a GaAs version has been developed (Hendrickson et al. (1987)), [26]. We worked on fabricating an equivalent Am2901 Josephson microprocessor because its capabilities can be compared directly with semiconductor microprocessors, enabling us to clarify the potential of Josephson circuit performance.

Semiconductor microprocessors usually have 16-word by 4-bit dual-port random access memory (RAM). However, in the Josephson microprocessor we developed (Figs. 14 and 15), we used a dual memory set of 64-bit RAM because dual-port RAM was difficult to implement. The microprocessor also features a dual memory set with a RAM shift register, 8-function ALU, Q register, and several controllers. The circuit is driven by three-phase power (ϕ_1, ϕ_2, and ϕ_3). Dual-rail logic was used in the arithmetic logic unit (ALU) and controllers, and the complementary signals are made from the input signals, with TI gates powered by ϕ_1. Decoding is done by gates powered by ϕ_1, memory reading is powered by ϕ_2, and data modification and writing are powered by ϕ_3. Both the minimum junction diameter and line width are 2.5 μm. Interconnecting lines are 4-μm wide. The chip includes 1841 MVTL gates.

The critical path of the carry signal is from the least to the most significant bit in the ALU, after which the sum signal is transferred from the ALU to RAM; 41 gates are required to sequentially switch along the path, with an interconnecting line 15 mm long. Operation of MVTL gates with a minimum junction diameter of 2.5 μm was confirmed with a gate delay below 10 ps in the ALU (Kotani et al. (1988)), [27]. The interconnection propagation delay was about 8 ps/mm. Thus, the microprocessor's critical path delay can be roughly estimated as 0.5 ns. Since the duty ratio of sinusoidal power is about 1/2, the maximum clock frequency was estimated as 1 GHz.

The critical current density of the fabricated Josephson junction is 2300 A/cm^2, higher than the optimum design value of 2100 A/cm^2. The measured operating margin was ±34% for

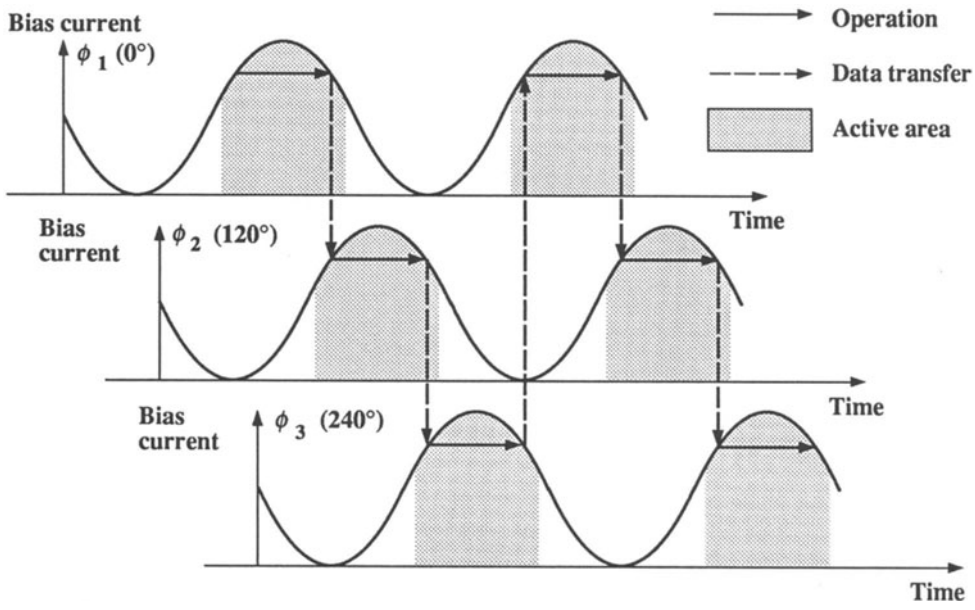


Fig. 13 Logic operation with a three-phase sinusoidal power supply.

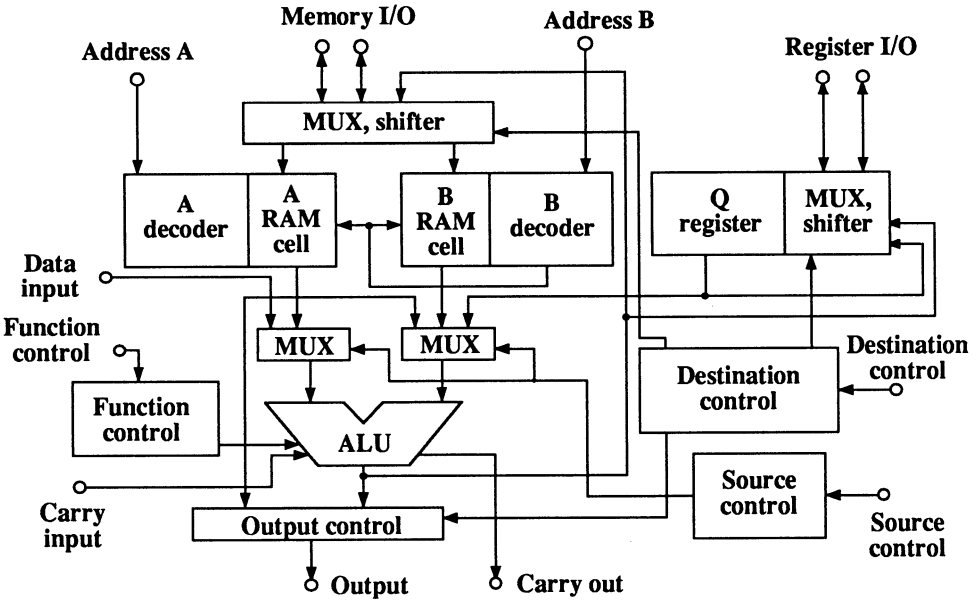


Fig. 14 Four-bit microprocessor schematic.

the OR gate and ±32% for the unit cell. All functions and source combinations were confirmed with an operating margin of ±16% at a clock frequency of 100 MHz, which is the word pattern generator's maximum clock frequency.

Operation along the critical path was tested using the high-speed pulse generator, with correct operation confirmed up to 770 MHz. The gate power dissipation was 3.6 μW/gate and the total power consumed by the chip was 5 mW. Microprocessor specifications and performance are summarized in Table 6.

The Josephson microprocessor operated at a clock frequency one order of magnitude faster and a power consumption three orders of magnitude less than semiconductor microprocessors. Table 7 compares Am2901 performance for silicon, GaAs, and superconducting materials.

6.2. 4-BIT PROCESSOR

The microprocessor was extended to a processor by adding a 4-bit multiplier, a 12-bit accumulator, 8-kbit instruction read-only memory (ROM), and a sequencer (Figs. 16 and 17). The minimum junction size was reduced from 2.5 μm to 1.5 μm, thus, downsizing the gates and memory cells. Consequently, the Am2901 microprocessor was reduced from 5 x 5 mm^2 to about 2 x 2 mm^2. All components were integrated on a 5 x 5 mm^2 chip. The total number of gates is 3056.

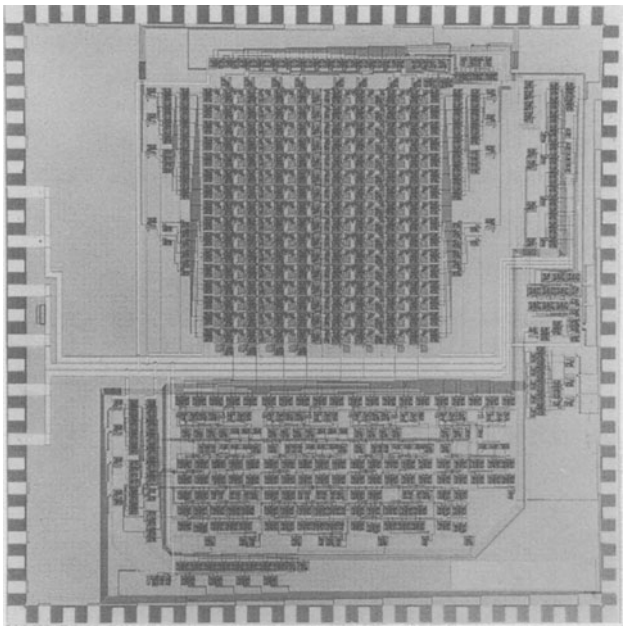
The ROM access time was 100 ps for the far-end ROM cell. The multiplication time was 200 ps for operation along the multiplier critical path. For the 4-bit microprocessor, we observed correct operation along the critical path up to a clock frequency of 1.1 GHz. The maximum clock frequency increased because the use of 1.5-μm junctions reduced the microprocessor's size. The chip's power dissipation was 6.1 mW. Because the ROM, multiplier, and microprocessor are operated by different phases of three pipelines, the ROM and multiplier are fast enough to be operated at a clock frequency of 1.1 GHz. Hence, the operating speed of the chip is only limited by the clock frequency of the microprocessor. Table 8 summarizes chip specifications and performance.

6.3. 8-BIT DSP

To achieve high-speed system performance, we designed an 8-bit DSP which includes a multiplier, ALU, instruction ROM, coefficient ROM, two data RAMs, and a sequencer (Fig. 18). The architecture is based on that of the Si DSP (Kikuchi et al. (1983)), [28]. Figure 19 shows the three-stage pipeline processing sequence. Both the 8-bit x 8-bit multiplier and 13-bit ALU are active in the third stage. Thus, the DSP completes once every machine cycle not only a series of multiply-add operations, but also a multiply-add operation using previously added data. This makes the data processing rate the same as the clock frequency.

Data memory consists of RAM A and RAM B, each in a 16-word by 8-bit configuration with its own addressing circuits. The instruction ROM (IROM) is 64 words by 24 bits. Each 24-bit instruction is divided into 7 fields. The DSP uses a special 16-word by 8-bit memory area (CROM) to store coefficients.

The DSP's I/O port consists of data registers and a controller. Output data is stored with an asynchronous external clock which interfaces the high-clock-speed Josephson DSP with low-clock-speed semiconductor systems.



1 mm

Fig. 15 (Left) Four-bit microprocessor chip, measuring 5 x 5 mm.

Table 6 Four-bit microprocessor

Specifications	
Gates	1,841
Josephson junctions	5,041
Minimum junction size	2.5 μm
Data RAM (2 sets)	16 word x 4 bit
ALU	4 bits, 8 functions
Chip size	5 x 5 mm
Performance	
Clock frequency	770 MHz
Power consumption	5 mW

Table 7 Comparison of Four-bit microprocessor performance

Device	Clock frequency (MHz)	Power dissipation (W)
Si bipolar	30	1.4
GaAs FET	72	2.2
Josephson junction	770	0.005

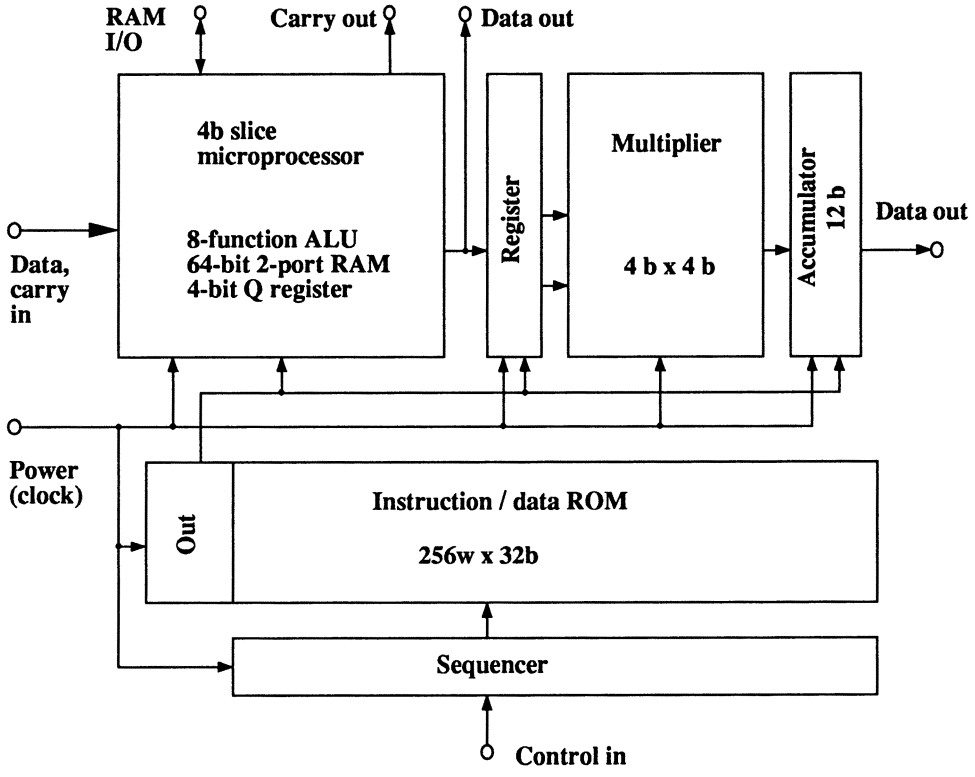


Fig. 16 Four-bit processor schematic.

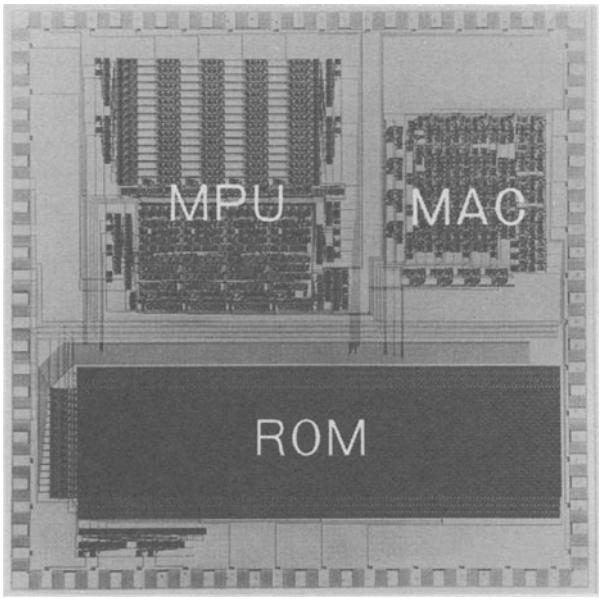


Fig. 17 (Left) Four-bit processor chip, measuring 5 x 5 mm.

Table 8 Four-bit processor

Specifications	
Gate	3,056
Josephson junction	24,000
Minimum junction size	1.5 μm
Instruction ROM	256 word x 32 bit
Data RAM	16 word x 4 bit x 2
ALU	4 bit, 8 functions
Multiplier	4 bit x 4 bit
Accumulator	12 bit
Chip size	5 mm x 5 mm
Performance	
ROM access time	100 ps
Multiplication time	200 ps
Microprocessor clock frequency	1.1 GHz
Power consumption	6.1 mW

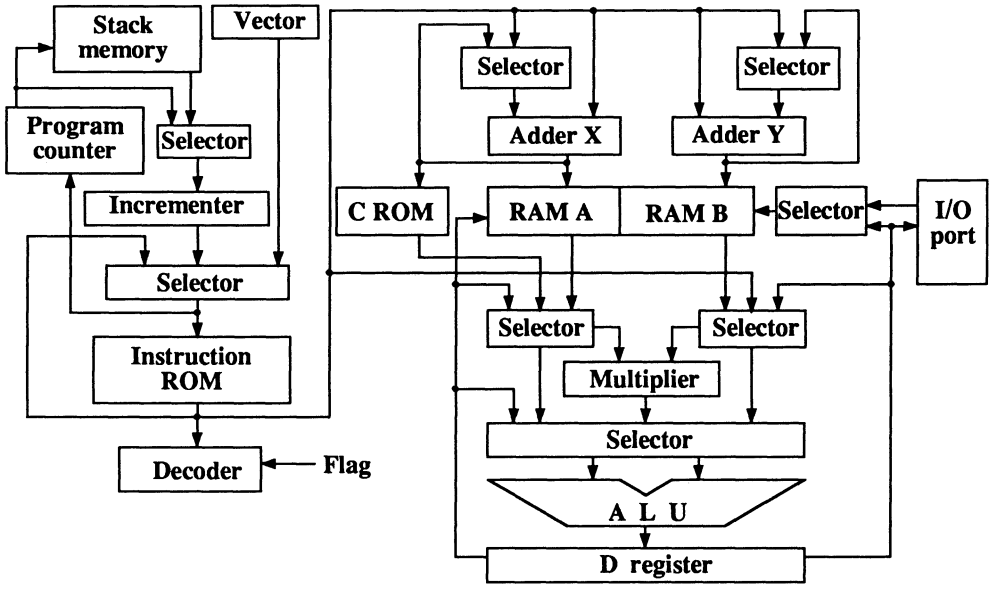


Fig. 18 Eight-bit DSP schematic.

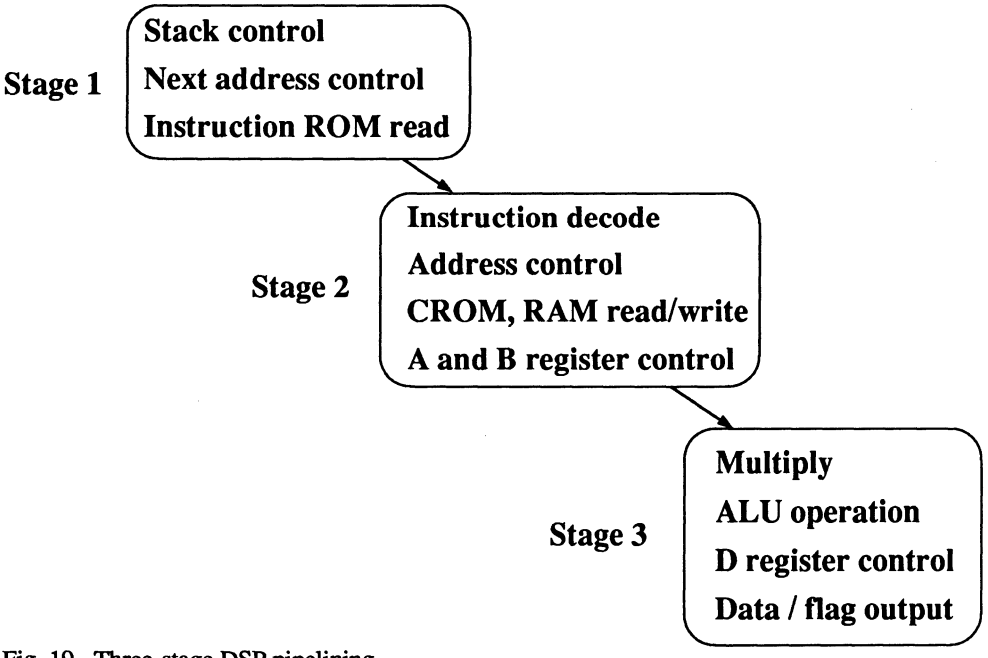


Fig. 19 Three-stage DSP pipelining.

Josephson 69 x 52 μm^2 logic unit cells, 26 x 16 μm^2 ROM cells, and 133 x 48 μm^2 data RAM cells are built into the DSP. The unit cell OR gate occupies 26 x 21 μm^2. Each data RAM cell stores data using superconducting persistent current, and has a sense amplifier to increase the operating margin. The minimum junction diameter is 1.5 μm and the minimum line width 2 μm. The two-layer superconducting interconnections are 3-μm wide with 2-μm spacing.

Figure 20 shows the DSP chip. To reduce the level of complexity, both the multiplier and ALU use ripple carry. The chip has 6300 gates and measures 5 x 5 mm^2.

We measured the operating speed of each circuit in the DSP. The carry propagation delay in the multiplier was 240 ps. Forty gates must switch sequentially along a 3.6-mm path. Because the propagation delay is 8 ps/mm, the average gate delay is estimated as 5.3 ps/gate. The delay for the ALU was 410 ps. In adder mode, the critical path in the ALU is the carry propagation route, and 44 gates must switch sequentially along the 4.2-mm path. The average delay is estimated as 7 ps/gate. The access time of the far-end IROM was 200 ps, and that of RAM cells was 130 ps.

We measured circuit speed, but not for all DSP operations because it was difficult to supply frequencies above 1 GHz and high bias current above 1 A. In actual operation, we were required to provide power with a transformer, which converts high-voltage, low-current power at room temperature to low-voltage, high-current power at low temperature. Even in that case, scattering of the critical current of junctions in the DSP should be decreased, because the total scattering at present is still too large to operate the DSP with the same bias-current level.

The internal clock cycle is limited by the third stage in the pipeline, where multiplication and addition are completed. The combined delay of the multiplier and ALU is 650 ps. The maximum clock frequency is estimated to be 1 GHz, which enables a nonparallel processing speed of 1 GOPS--100 times faster than the conventional CMOS DSP - obtained using about one tenth the power consumption of the chip (Kotani et al. (1990)), [23]. Table 9 summarizes chip specifications and performance.

6.4. MEMORY

JJ memory circuits of 1 kbit to 4 kbit have been reported (Tahara et al. (1991), Suzuki et al. (1989), Nakagawa et al. (1989), and Kurosawa et al. (1990)), [10, 11, 29, 30], and their performance is summarized in Table 10.

This section focuses on a memory circuit with a capacitively-coupled cell (Suzuki et al. (1989)), [11]. In such a cell, one bit of information is stored as a flux quantum Φ_0, caused by superconducting persistent current in an RF SQUID, which is a superconducting loop with one Josephson junction. Our cell consists of an RF SQUID, a sense junction, and two capacitors (Fig. 4 (d)). A memory cell is selected by two magnetically-coupled x- and y-address lines. Positive (logic 1) or negative (logic 0) current pulses are applied to these address lines, causing one or zero flux quantum to be stored in the SQUID. Information is capacitively coupled from the SQUID to the sense junction. In reading, a negative-polarity address current pulse is applied and the sense junction is biased below the critical current. When Φ_0 is stored, the SQUID changes from the one to the zero flux quantum state. A small pulse appears across the junction when the state is changed. The pulse voltage multiplied by the pulse width almost equals the flux quantum value Φ_0. For example, a 10-ps pulse of 200 μV across the junction is transferred

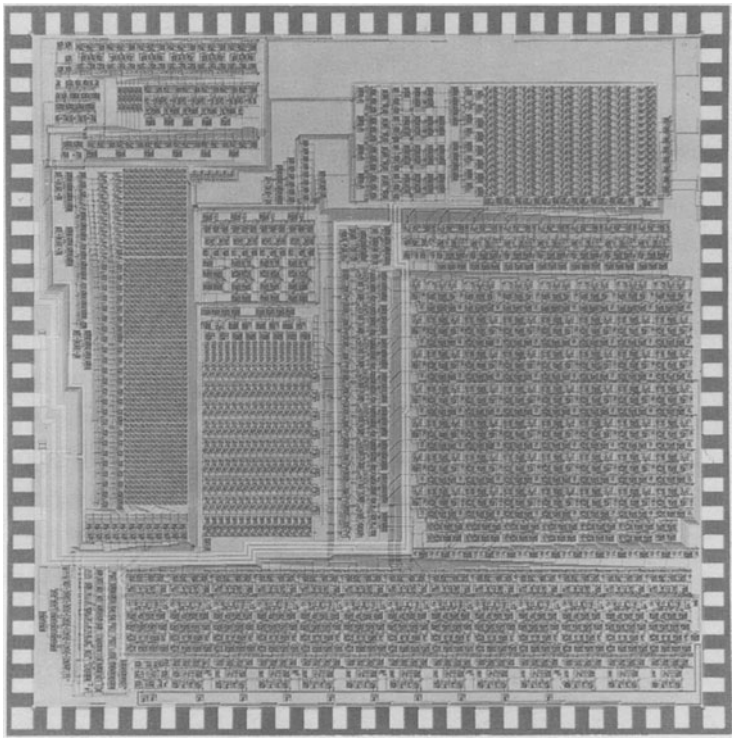


Fig. 20 (Left) Eight-bit DSP chip, measuring 5 x 5 mm.

Table 9 Eight-bit digital signal processor

Specifications	
Gates	6,300
Josephson junctions	23,000
Minimum junction size	1.5 μm
Instruction ROM	64 word x 24 bit
Coefficient ROM	16 word x 8 bit
Data RAM (2 sets)	16 word x 8 bit
ALU	13 bits, 16 functions
Multiplier	8 x 8 bits
Chip size	5 x 5 mm
Performance	
Instruction ROM access time	200 ps
Data RAM access time	130 ps
Multiplication time	240 ps
Adding in ALU	410 ps
Power consumption	12 mW
Estimated internal clock frequency	1 GHz

to the sense junction, causing a sense-junction voltage transition. Although reading is destructive, it is followed immediately by rewriting.

The decoder was constructed using specially designed AND gates. To reduce the number of logic stages needed for decoding, an AND gate with a fan-out of 4 was developed. A 6-bit to 64-bit address decoder can be constructed with three stages of these AND gates. The operation of the 6-to-64 decoder was confirmed with a decoding time of 90 ps.

Memory cells are arranged in a 64-by-64 configuration, so each driver gate must drive 64 cells connected in series. To increase gate drivability, we introduced a new driver gate that generates a voltage exceeding the gap voltage. The driver gate has two parallel branches of four junctions in series with one resistor. Bias current is supplied to the gate between the two branches. The junction critical current and resistance were designed to be equal for both branches and also chosen so that the driver circuit can drive the 64 memory cells. The rise time measured at the far end of the drive line was 60 ps.

Figure 21 shows the 4-kbit memory designed and fabricated with the above circuits. The minimum junction diameter is 2.5 μm and the minimum line width 4 μm. Each memory cell measures 83 x 83 μm^2. A rather large cell was used to verify memory circuit feasibility without requiring sophisticated process technology. The 7.7 x 7.7 mm^2 chip has 14468 junctions. Although the chip was not fully functional, the measured access time was 590 ps and power dissipation was 19 mW. Table 11 summarizes chip specifications and performance.

Now that it is possible to make 1-kbit to 4-kbit Josephson memory, it may be possible to extend circuits to between 16 kbits and 64 kbits by improving fabrication techniques. Because of poor gate drivability, however, it is very difficult to develop high-density memory, e.g., 1 megabit. To increase density, we must decrease cell size and wiring line width. Unfortunately, reducing wiring width increases the driver gate's output line inductance, which may increase access time beyond that of semiconductor memory. Thus, fabrication methods for high-density memory remain unclear.

7. Interfacing

Josephson logic operates at a clock frequency above 1 GHz and its logic swing is less than 3 mV. Two factors dictate the need for interfaces between Josephson and semiconductor devices. One is the need for level shifting of the Josephson 3-mV logic swing to the 1 V required to drive semiconductor logic (Suzuki et al. (1988)), [31]. The other is the conversion of the clock frequency from 1 GHz to 100 MHz. Simply reducing the clock frequency causes information to be lost in a Josephson system. This can be avoided by using a serial-to-parallel converter (Ohara et al. (1989)), [32]. These two interface circuits are described here.

7.1. HIGH-VOLTAGE DRIVER

The output of a Josephson logic gate, determined by the junction's gap voltage, is only 2.8 mV for Nb/AlOx/Nb junctions. It would seem easy to use series-connected junctions to obtain a voltage higher than the gap voltage, but this is true only for series-connected junctions without a load resistor. Even in such a case, critical current scattering should be small. When a load resistor is connected to series-connected junctions, the junctions do not switch simultaneously. A voltage step occurs for each junction switched to the voltage state.

Table 10 Josephson memory performance

Organization	Chip size (mm^2)	Cell type	Readout mode	Access time (ps)	Power (mW)	Reference
1K x 1-bit	36.0	Henkels	NDRO	570	13.0	29
256 x 4-bit	10.0	Variable threshold	NDRO	500	1.9	30
4K x 1-bit	36.0	Vortex transition	NDRO	580	6.7	10
4K x 1-bit	59.3	Capacitively coupled	DRO	590	19.0	11

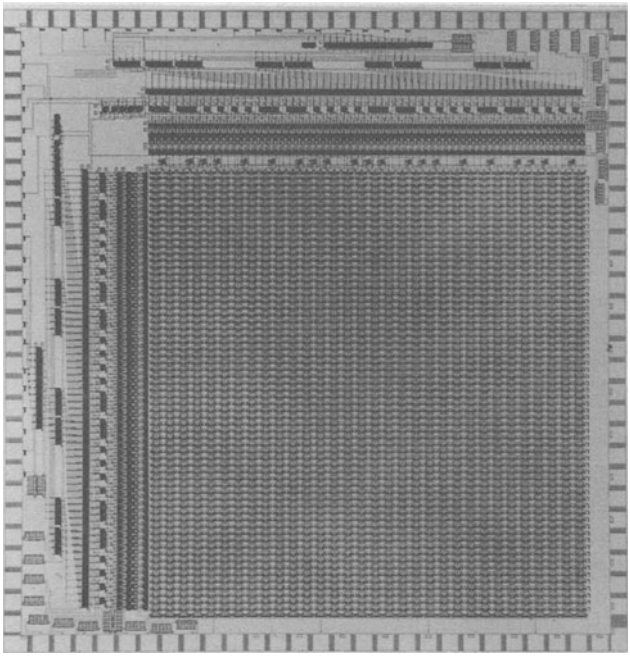


Fig. 21 (Left) Four-kbit memory chip, measuring 7.7 x 7.7 mm.

This problem was solved by connecting two sets of series-connected junctions in parallel. Junctions connected this way switch simultaneously and produce an output voltage much higher than the junction gap voltage.

We designed a high-voltage gate with 52 junctions in each branch to build a Josephson driver gate, and obtained an output voltage of 150 mV (Suzuki et al. (1988)), [31]. The circuit used to test the output interface is shown in Fig. 22 (Suzuki et al. (1990)), [33]. Output voltage from the 4JL gate was amplified to 150 mV with the Josephson driver and further amplified by a GaAs comparator immersed in liquid helium. We obtained an output voltage of 1.7 V from the comparator. The output interface circuit operated with a clock frequency up to 800 MHz.

7.2. SERIAL-PARALLEL CONVERTER

We designed an 8-bit serial-parallel converter (Ohara et al. (1989)), [32] consisting of an 8-bit shift register and a divide-by-eight prescaler that generates a pulse every eight clock cycles. The converter contains 92 MVTL gates. A divide-by-two prescaler generates a pulse when the number of input pulses is even, i.e., it outputs one pulse for every two inputs. Cascading three divide-by-two prescalers forms the divide-by-eight prescaler. Using this circuit, we confirmed serial-to-parallel conversion up to 1.3 GHz. That is, the 1.3-GHz Josephson output was divided into an 8-bit parallel signal with 160 MHz operation.

8. Hybrid System

Josephson LSI technology has progressed remarkably in the last several years, with all of the components required to fabricate a Josephson computer now available. Integration densities, however, remain lower than those of silicon, making fabrication of a practical high-speed Josephson computer difficult. To overcome this difficulty, a way must be found to apply existing Josephson LSI technology. One candidate may be a hybrid of Josephson and semiconductor devices, in which Josephson circuits are used to accelerate computation.

Josephson circuits have been considered for all high-speed computer components, i.e., the central processing unit (CPU), cache memory, and main memory (Anacker (1979)), [34]. Chips remain experimental, however, hobbled by the yet immature technology. The massive investment needed to spur mass production cannot be expected before a Josephson computer becomes marketable, however. This is the catch-22 that must be resolved before Josephson technology will take hold.

As suggested above, the development of a practical pure-Josephson computer may well be preceded by a hybrid consisting of both Josephson and semiconductor devices. This will be useful only if the distances between Josephson and semiconductor devices are very short--otherwise, signal propagation between device types will introduce delays that would eliminate any high-speed advantage of the Josephson device. Attempts to build such a hybrid have focused on a conventional cryostat, into which signal lines are inserted through the top of the chamber. This, however, requires about one meter of cable and causes a delay of several nanoseconds, making costly demands on the timing budget. This problem rules out use of a conventional cryostat. In response ,we developed a cryostat system (Fig. 23) that enables Josephson devices to be located only a few centimeters away from room-temperature peripherals (Kotani et al. (1991)), [35].

Table 11 Four-kbit memory

Specifications	
Organization	4K x 1-bit
Josephson junctions	14,468
Cell size	83 x 83 μm
Chip size	7.7 x 7.7 mm

Performance	
Access time	590 ps
Power consumption	19 mW

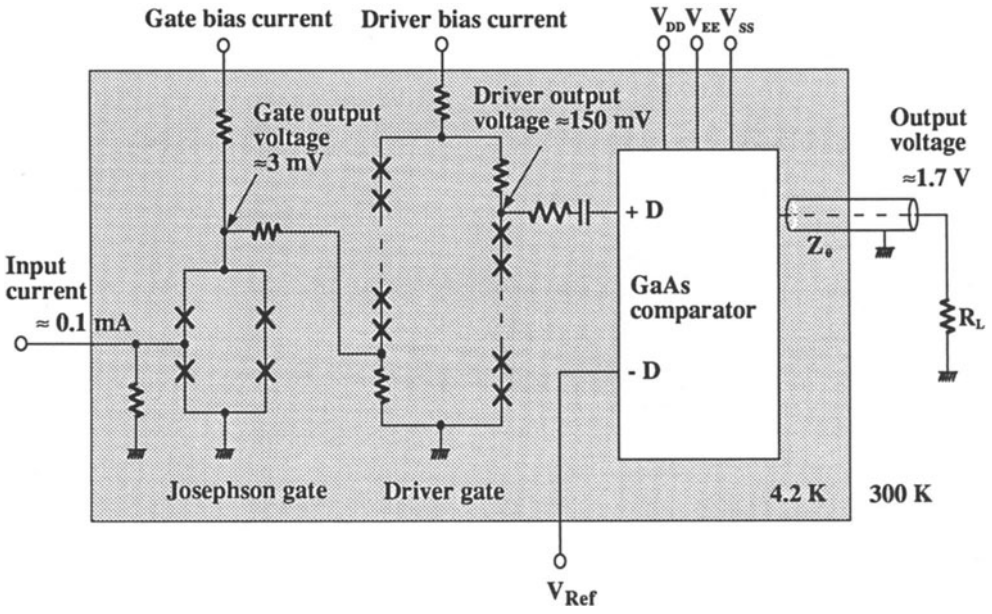


Fig. 22 Equivalent circuit for testing an output interface consisting of a 4 JL Josephson gate, a driver gate, and a GaAs comparator.

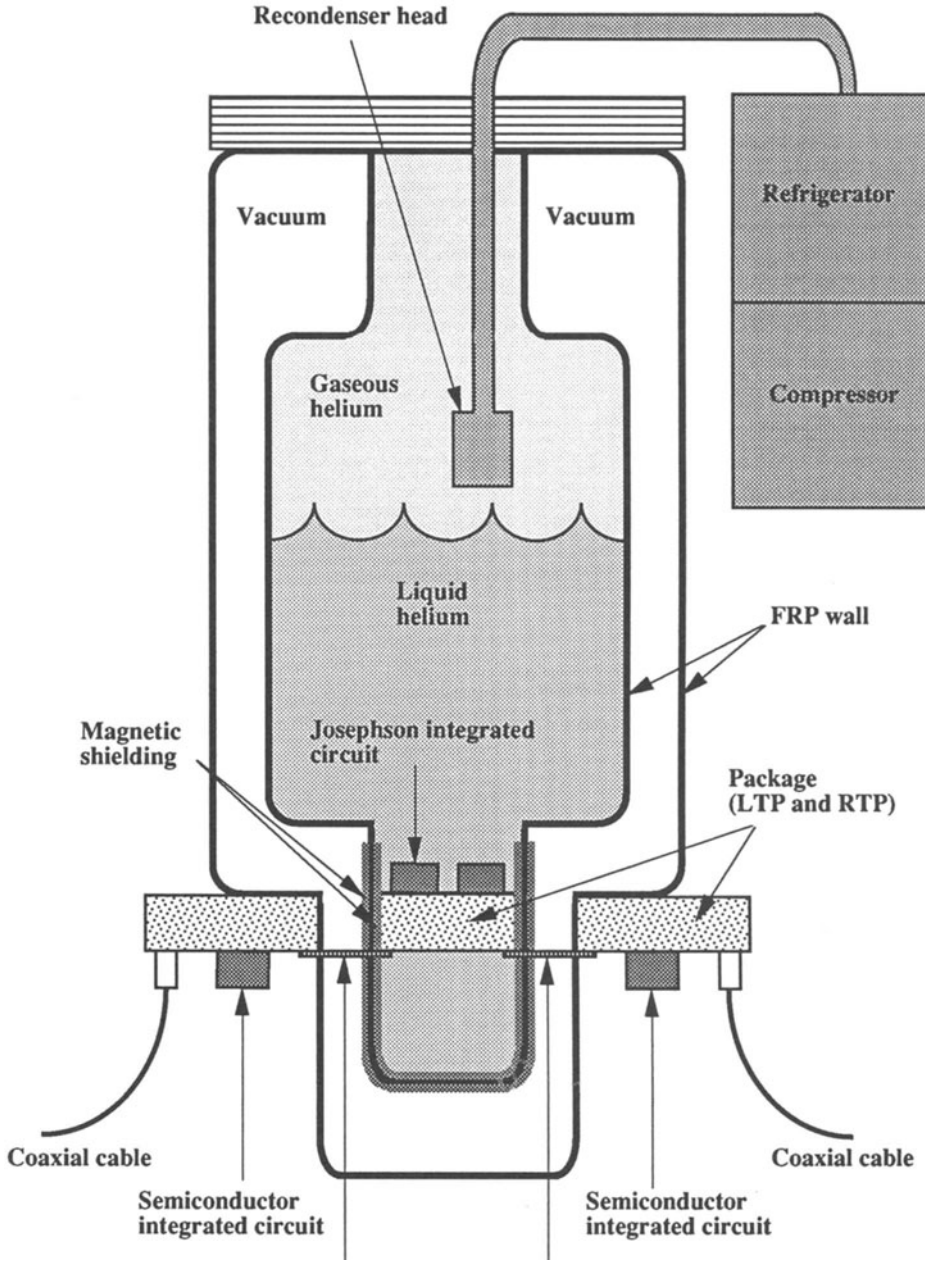


Fig. 23 Cryostat cross section.

Flexible cables are passed through the insulated fiber-reinforced plastic (FRP) wall of the chamber, shortening the signal propagation distance to 24 mm to relieve the transmission bottleneck between Josephson circuits and room-temperature peripherals. Signals are transmitted through polyimide flexible cable (PFC) that penetrates the vacuum wall between the low-temperature (LTP) and room-temperature packages (RTP). Double magnetic shielding is used in this cryostat, one inside the chamber and the other inside the vacuum wall. When the cryostat is connected to a refrigerator, helium evaporated due to heat generation in the cryostat is reliquefied by the cooled recondenser head. The cryostat can be operated in a closed-cycle mode without externally supplied liquid helium. A flexible laminated copper-plated polyimide film cable with 30 signal lines connects the LTP and RTP packages and is fixed in place by epoxy adhesive at slits cut into the FRP wall. The most difficult problem was to pass cables through the chamber wall while retaining the insulating vacuum and minimizing heat conduction.

The cryostat was combined with a 3-watt refrigerator. We placed two PFCs in this cryostat so that we could use 60 signal lines. Heat conducted through the cables totals 1.2 W, and that lost through the cryostat wall totals 1.5 W. Since a typical Josephson chip dissipates 5 to 20 mW, we can install a large number of the chips in the 3-watt refrigerator.

The propagation delay through the connection cables of the 24-mm package was 130 ps, about a hundredth of the cable delay in a conventional cryostat. To verify system reliability, we installed a 4-bit microprocessor that operated up to a clock rate of 1.1 GHz, although it had been operated up to 770 MHz in the conventional cryostat described in the previous section. The improved operating frequency was due to improved packaging. Note that refrigerator noise was suppressed sufficiently to enable chips to operate reliably.

This cryostat system makes integration of Josephson devices and semiconductor electronics possible. Even though the chip integration density remains low, this is more than compensated by the high speeds at which the system operates. We have demonstrated a cryostat for liquid helium--a cryostat for liquid nitrogen would be much easier to fabricate. We can thus introduce the concept of a variety of devices operating at different temperatures installed on the same circuit board. For example, Josephson devices at 4.2 K, CMOS at 77 K, and bipolar devices at room temperature may be used in the same system, each operating in its most suitable signal processing environment.

We demonstrated the cryostat for a hybrid system. To make a practical hybrid system using this cryostat, we must develop more sophisticated packaging.

9. Future Directions

As described above, Josephson LSI technology has progressed markedly. Microprocessors with a few thousand gates and 1- to 4-kbits of memory are feasible, even though they are still experimental. To compete with semiconductor circuits, a large-scale Josephson circuit, such as a 16-bit or 32-bit processor will have to be developed--not yet possible using current techniques, however.

An interim answer that could help get Josephson devices the market support needed to finance the required advances in technology is development of practical, attractive applications possible at the present level of technology--no easy task, since almost all high-speed signal processing can be attained in parallel processing with conventional silicon processors. Ten processors operating in parallel, for example, can achieve the same speed as the Josephson processor. There are, however, some high-speed applications which cannot be attained by

parallel processing of conventional semiconductor processors, e.g., the infinite-impulse-response (IIR) filter, in which preceding data is used for subsequent calculation. The microprocessors operating at a clock rate of 1 GHz required for such an application can not be realized with semiconductor devices.

It is also important to apply existing technology to low-temperature electronics. One such candidate could be a signal processing circuit for a multichannel SQUID system expected to be used in medical diagnosis. The simplest signal processing is by a multiplexer. A single-chip SQUID (Fujimaki et al (1988)), [36], in which signals are treated as digital rather than analog, is especially suitable for multiplexing the signals from a multichannel system because the signals are compatible with those in Josephson digital circuits. By multiplexing the output signals from the single-chip SQUID, we can obtain time-shared signals at room temperature through a single output line (Gotoh et al. (1991)), [37]. Josephson processors would also be useful for the more complicated data processing of a multichannel system exceeding 200 channels. The first step toward such a practical system would appear to be a processor, such as a SQUID processor, that handles signals generated at low temperatures. The key to such a system would be a cryostat (as described above).

Whether the question is one of the density or speed, or even of technology, the major point is to demonstrate a Josephson digital system that is clearly more useful in its application than any other signal processing technology. Once this usefulness is understood and recognized, the market for Josephson-based superconducting electronics will be opened.

If the market grows as hoped, a hybrid computer integrating Josephson devices at 4.2 K and low-temperature CMOS at 77 K may become a reality. In such a computer, parallel computation would relegate massive calculation to CMOS processors and high-speed calculation to the Josephson processor. Such a system would further promote development of the technology needed for a large-scale Josephson computer.

The possibility that Josephson junctions made from high-T_C materials will find use as components in high-speed computers is made questionable by the fact that a high-T_C junction consumes over one hundred times the power required by a niobium junction (Hasuo and Imamura (1989)), [38]--suggesting that, if anywhere, high-T_C junctions may prove valuable for small-scale applications such as SQUIDs, rather than ever being widely used as basic computer elements. Table 12 summarizes the anticipated performance of Josephson latching logic gates operated at 77 K, compared with that of Nb/AlOx/Nb-junction gates at 4.2 K. The operating voltage is proportional to the superconducting material's critical temperature, T_C. The T_C of Nb is 9.2 K, and its operating voltage is about 3 mV. Thus, $YBa_2Cu_3O_x$ with a T_C of 90 K would operate at 30 mV. The operating current should be proportional to the operating temperature; otherwise, logic gates will malfunction due to thermal noise. The operating speed is determined primarily by the RC time constant as described in Section 2, where R is the stripline impedance, and C is the junction capacitance. R is usually chosen to match the tunneling resistance. C depends on the dielectric constant and the thickness of the tunneling barrier, so its value varies with the barrier material. We do not yet know which tunneling barrier is best for a high-T_C material. As a first step, we assume an AlOx barrier. As described, the current should be increased 20 times in high-T_C materials by increasing the current density, not by increasing the junction area. Otherwise, C increases and the switching speed decreases. The value of R remains unchanged because both voltage and current increase by the same amount. Therefore, the switching speed of gates made of high-T_C materials is almost the same as that of Nb/AlOx/Nb junctions.

Table 12 JJ performance at 4.2 K and 77 K

	Nb at 4.2 K	High-T_C at 77 K	Ratio
Voltage	≈3 mV	≈30 mV	10
Current	0.1 - 0.5 mA	2 - 10 mA	20
Power	1 -10 μW/gate	0.2 - 2 mW/gate	200
Switching time	1 -10 ps/gate	1 -10 ps/gate	1

It is apparent that the performance of the Josephson logic gate is not improved by using high-T_C materials, and device performance is not generally improved by increasing the operating temperature. At lower temperatures, one obtains better performance. This suggests that the future direction of high-speed LSI logic and memory devices is toward lower temperatures.

10. Conclusion

This paper has described techniques for developing and fabricating Josephson microprocessors: niobium-junction fabrication, high-speed gate families, and the three-phase power supply. Niobium junctions are stable and reliable, easier to fabricate than semiconductor devices, and provide uniform characteristics. The high-speed gate families are important for constructing high-speed processors. The MVTL gate family attains sub-10 ps gate delays, even when loaded. Three-phase power also supports high-speed processor operation because it needs no latch circuit for storing information during power-off periods. These techniques make it feasible to construct high-speed microprocessors operating at a clock frequency of around 1 GHz.

Despite the great potential of Josephson microprocessors, their present limits in integration prevent them from being practical. It is very important now to find a market where small-scale Josephson microprocessors can drastically improve performance over that of conventional semiconductor technology. It is essential to carefully cultivate the field of superconducting electronics. Applying Josephson microprocessors to an existing use, such as a multichannel SQUID system, may prove useful for this purpose.

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